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10-30-98
PATENT
P54508

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Hae-Seung LEE

Serial No.: 08/931,125

Examiner: *TO BE ASSIGNED*

Filed: 16 September 1997

Art Unit: *TO BE ASSIGNED* 2751

For: MEMORY SYSTEM FOR IMPROVING DATA INPUT/OUTPUT PERFORMANCE
AND METHOD OF CACHING DATA RECOVERY INFORMATION

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. §1.56, and §§1.97(c) and 1.98 as amended, applicant cites,
provides a copy and discusses the following art reference:

1. U.S. Patent No. 5,341,381 to Fuller, issued 8/94

As noted, Fuller '381 discloses a redundant array parity caching system.

The citation of the foregoing references is not intended to constitute an assertion that other
or more relevant art does not exist. Accordingly, the Examiner is requested to make a wide-
ranging and thorough search of the relative arts.

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No fee is incurred by this Statement.

Respectfully submitted,

Robert E. Bushnell 34973
For Robert E. Bushnell
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